BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :
H05K 3/30, H01B 17/00
H01L 39/02, H05K 7/02, 7/10

A1

(11) International Publication Number: WO 90/13991

(43) International Publication Date: 15 November 1990 (15.11.90)

(21) International Application Number: PCT/US90/01828

(22) International Filing Date: 9 April 1990 (09.04.90)

(30) Priority data:
345,280 1 May 1989 (01.05.89) US

(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

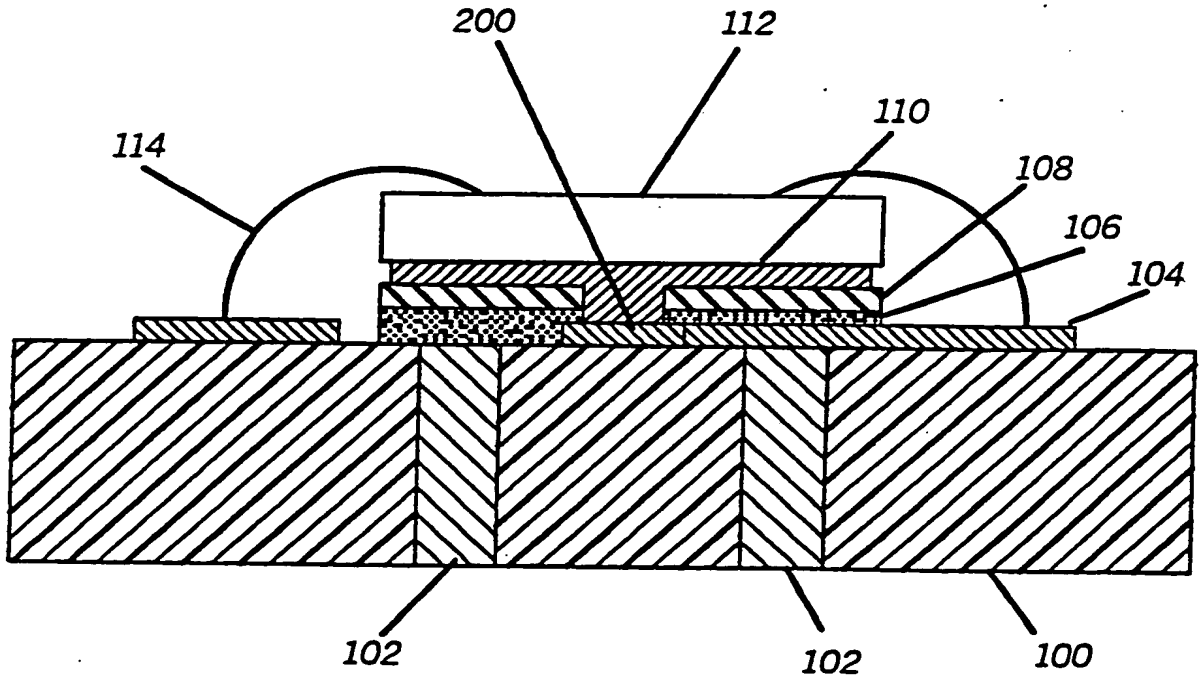
(72) Inventors: FREYMAN, Bruce, J. ; 2641 N.W. 62nd Terrace, Sunrise, FL 33313 (US). MILES, Barry, M. ; 9304 Chelsea Drive South, Plantation, FL 33324 (US). JUSKEY, Frank, J. ; 4103 N.W. 69th Terrace, Coral Springs, FL 33065 (US).

(74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(81) Designated States: AT (European patent), BE (European + patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
With amended claims.

(54) Title: METHOD OF GROUNDING AN ULTRA HIGH DENSITY PAD ARRAY CHIP CARRIER



(57) Abstract

A die pad (108) with a punched hole providing a throughway (110) is affixed upon the chip carrier base (100). Such throughway permits the electronic interconnection of the die backside (112) to a conductive runner (104) by means of electrically conductive material (110) set between the die backside (112) and the conductive runner (104).

DESIGNATIONS OF "DE"

Until further notice, any designation of "DE" in any international application whose international filing date is prior to October 3, 1990, shall have effect in the territory of the Federal Republic of Germany with the exception of the territory of the former German Democratic Republic.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MC	Monaco
AU	Australia	FI	Finland	MG	Madagascar
BB	Barbados	FR	France	ML	Mali
BE	Belgium	GA	Gabon	MR	Mauritania
BF	Burkina Faso	GB	United Kingdom	MW	Malawi
BG	Bulgaria	GR	Greece	NL	Netherlands
BJ	Benin	HU	Hungary	NO	Norway
BR	Brazil	IT	Italy	RO	Romania
CA	Canada	JP	Japan	SD	Sudan
CF	Central African Republic	KP	Democratic People's Republic of Korea	SE	Sweden
CG	Congo			SN	Senegal
CH	Switzerland	KR	Republic of Korea	SU	Soviet Union
CM	Cameroon	LI	Liechtenstein	TD	Chad
DE	Germany, Federal Republic of	LK	Sri Lanka	TG	Togo
DK	Denmark	LU	Luxembourg	US	United States of America

METHOD OF GROUNDING AN ULTRA HIGH DENSITY PAD ARRAY CHIP CARRIER

Technical Field

This invention relates generally to a method of making an ultra high density pad array chip carrier, more particularly a method for grounding of an integrated circuit (I.C.) device in ultra high density pad array chip carriers.

Background Art

Grounding ultra high density chip carrier assemblies typically requires a wire bond from a conductive runner acting as ground on a substrate to a metallized polyimide film die pad. Wire bonding in chip carrier assemblies is disadvantageous due to the larger die pad size required to bond the wire, larger production and material costs, and lower current carrying capacities of typical bond wires such as a gold bond wire.

Eliminating wire bonding to metallized polyimide film die pads reduces several undesirable effects. First, wire bonding requires a larger die pad to allow a wire bonder to place a wire

next to the die on the metallized polyimide film die pad. Further, polyimide film (as opposed to metallized alumina) produces poor wire bonds due to its compliant nature. Additionally, eliminating wire bonds permits the elimination of the metal layer on the polyimide die pad, since no wire bonding to the die pad is necessary. Wire bonding requires the operator to change the wire bonder parameters, such as, from a ceramic chip carrier profile to a polyimide film profile in order to make a reliable bond. Grounding a high power integrated circuit device with a wire bond from a polyimide film die pad to a conductive runner is an ineffective method of semiconductor grounding due to the insufficient current carrying capacity of typical bond wires. Disposing of the grounded wire bond by means of the present invention reduces production costs and production time, while increasing the efficiency and effectiveness of the chip carrier assembly.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a method for grounding the backside or bottom of a semiconductor die to a chip carrier base overcoming the detriments discussed above.

Briefly, according to the invention, a die pad constructed of a suitable dielectric material has a hole formed therein, so as to provide a throughway between its top and bottom surfaces. This die pad is affixed to the chip carrier base. The throughway permits the interconnection of the bottom surface of the die to a conductive runner by means of an electrically conductive material.

Brief Description of the Drawings

Figure 1 illustrates a top plan view of the chip carrier with a typical pattern of conductive areas.

Figure 2 illustrates a cross section of the chip carrier, die pad, and semiconductor die in accordance with the present invention.

Figure 3 illustrates a top plan view of the chip carrier base with the die pad placed on top of the chip carrier base in accordance with the present invention.

Detailed Description of the Preferred Embodiment

Referring to Figure 1, there is shown an alumina ceramic substrate 100 having conductive areas (or metal runners) (104) deposited thereon. Some of these conductive areas terminate at a metal land (200) that serves as a common grounding point. Preferably, the metal land comprises a square having a size dependent on the design of the substrate, although other shapes may be used. According to the invention, a convenient size of .020 inches X .020 inches (.051cm X .051cm) facilitates assembly. The metal land 200 is positioned directly below the through-hole in the die pad (108) shown in Figure 2.

Referring to Figure 2, the die pad (108) is affixed to at least a portion of the conductive areas (104) by means of an effective amount of adhesive, preferably Pyralux acrylic adhesive (106) made by Dupont. The die pad (108), either metallized or unmetallized, comprises of a polyimide film .002 inches (.005cm) thick, and laminated with .001 inch (.003cm) Dupont Pyralux modified acrylic adhesive (106). Before the die pad is tacked onto the substrate, a hole, (preferably .020 inches (.051cm) to .100 inches (.255cm) in diameter) is formed in the polyimide film die pad and the attached Pyralux acrylic adhesive. This hole is positioned in the die pad (106) so as to mount over the grounded metal land (200) on the ceramic substrate (100). Optimally, the solder filled throughholes (102) may be electronically connected to the conductive areas of the substrate (104) as is known in the art.

Referring to figures 2 and 3, the die pad and acrylic adhesive is then positioned on the substrate, which is then laminated. The lamination process causes an intimate bond between the die pad (108), the acrylic adhesive (106) and the conductive areas (104).

Preferably, a conductive material (110) comprising silver filled epoxy flows through the through-hole formed in the die pad

(108) and acrylic adhesive (106) to make contact with the grounded metal land (200) on the substrate (100). The silver filled epoxy is also dispensed onto the top surface of the die pad, creating an electronic connection between the bottom surface of the die (112) and the grounded metal land (200) when the die (112) is placed into the epoxy in an assembly process.

Finally, wire bonds (114) may be connected from various conductive areas (104) on the substrate to the semiconductor die 112.

What is claimed is:

Claims

1. A chip carrier assembly comprising:

a semiconductor chip;

a substrate including at least one conductive area;

a nonconductive die pad carried by the substrate having at least one passage therethrough, and being positioned between the semiconductor and the substrate; and

an electrically conductive material, located in said passage and between the substrate and the semiconductor chip for providing electrical interconnection between the semiconductor chip and said one conductive area of the substrate.

2. A chip carrier assembly as defined in claim 1, wherein said substrate comprises an ceramic chip carrier base.

3. A chip carrier assembly comprising:

a semiconductor chip;

a substrate including at least one conductive area;

a polyimide film die pad carried by the substrate having at least one passage therethrough, and being positioned between the semiconductor and the substrate; and

an electrically conductive material, located in said passage and between the substrate and the semiconductor chip for providing electrical interconnection between the semiconductor chip and said one conductive area of the substrate.

4. The chip carrier assembly as defined in claim 1, wherein said electrically conductive material comprises conductive metal filled epoxy.

5. The chip carrier assembly of claim 4, wherein said conductive metal filled epoxy comprises silver.

6. A chip carrier assembly comprising:

a semiconductor chip;

an alumina ceramic substrate including conductive areas;

a polyimide film die pad carried by the substrate having at least one passage therethrough, and being positioned between the semiconductor and the substrate, and

an electrically conductive silver filled epoxy, located in said passage and between the substrate and the semiconductor chip for providing electrical interconnection between the semiconductor chip and and said one conductive area of the substrate.

7. A chip carrier assembly for mounting a semiconductor chip comprising:

a semiconductor die;

a chip carrier base including metallic runners;

a nonconductive die pad with at least one pathway carried by the chip carrier base and positioned between the semiconductor die and said carrier base;

electrically conductive material interconnecting said semiconductor die and at least one of said metallic runners through said pathway in said die pad.

8. A chip carrier assembly for mounting a semiconductor chip comprising:

a semiconductor die;

a chip carrier base including metallic runners;

a polyimide film die pad with at least one pathway carried by the chip carrier base and positioned between the semiconductor die and said carrier base;

electrically conductive material interconnecting said semiconductor die and at least one of said metallic runners through said pathway in said die pad.

9. The chip carrier assembly of claim 7, wherein said chip carrier base comprises ceramic alumina.

10. The chip carrier assembly of claim 7, wherein said electrically conductive material comprises silver filled epoxy.

11. The chip carrier assembly of claim 7, wherein said pathway comprises a punched hole therethrough said die pad positioned directly above said conductive runner.

12. A method for constructing a chip carrier assembly, comprising the steps of:

(a) preparing a ceramic base;

(b) laminating the die pad with an acrylic adhesive at a temperature so that the adhesive attaches to the die pad but does not begin to cure and punching a hole through said die pad and attached acrylic adhesive;

(c) tacking said die pad onto a preheated ceramic base, positioning said punched hole in the die pad directly over a grounded conductive runner, forming a die pad bonded assembly;

(d) heat laminating said die pad bonded assembly to fully cure the acrylic adhesive;

(e) dispensing silver filled epoxy onto the middle of said die pad, forcing said silver filled epoxy through the said passway in the die pad so as to form an electronic connection between the die, which is placed into the epoxy, and said conductive runners.

(f) placing the die onto the silver filled epoxy, thereby forming an electronic connection between the backside of the die and the conductive runners.

13. A method for grounding a semiconductor through a chip carrier assembly, comprising the steps of:

(a) providing a substrate having metallized areas;

(b) applying an adhesive to a polyimide film die pad at a temperature that causes the adhesive to adhere to the die pad without curing;

(c) punching a hole through both the die pad and uncured acrylic adhesive in a position wherein said hole will be located over a metallized area on said substrate;

(d) tacking said die pad onto a substrate, positioning said punched hole in the die pad directly over a grounded conductive runner, forming a die pad bonded assembly;

(e) heat laminating said die pad bonded assembly to fully cure the acrylic adhesive;

(f) dispensing silver filled epoxy onto the middle of said die pad, forcing the silver filled epoxy through the said punched hole in the die pad so as to form an electronic connection between the die, which is placed into the epoxy, and said conductive runners.

AMENDED CLAIMS
[received by the International Bureau on 10 October 1990 (10.10.90); riginal claims 1, 3, 7, 8 and 11 amended ; other claims unchanged (5 pages)]

1. A chip carrier assembly comprising:

a semiconductor chip, having a bottom surface;

a substrate including at least one conductive area;

a nonconductive die pad intimately bonded to at least one of the conductive areas of the substrate having at least one passage therethrough, and being positioned between the semiconductor chip and the substrate; and

an electrically conductive material, located in said passage and between the substrate and the semiconductor chip, for providing electrical interconnection between the semiconductor chip bottom surface and said one conductive area of the substrate.

3. A chip carrier assembly comprises:

a semiconductor chip, having a bottom surface;

a substrate including at least one conductive area;

a polyimide film die pad intimately bonded to at least one of the conductive areas of the substrate having at least one passage therethrough, and being positioned between the semiconductor chip and the substrate; and

an electrically conductive material, located in said passage and between the substrate and the semiconductor chip, for providing electrical interconnection between the semiconductor chip bottom surface and said one conductive area of the substrate.

7. A chip carrier assembly for mounting a semiconductor chip comprising:

a semiconductor die, having a bottom surface;

a chip carrier base including metallic runners;

a nonconductive die pad with at least one pathway intimately bonded to at least one of the metallic runners on the chip carrier base and positioned between the semiconductor die and said carrier base;

electrically conductive material interconnecting said semiconductor die bottom surface and at least one of said metallic runners through said pathway in said die pad.

8. A chip carrier assembly for mounting a semiconductor chip comprising:

a semiconductor die, having a bottom surface;

a chip carrier base including metallic runners;

a polyimide film die pad with at least one pathway intimately bonded to at least one of the metallic runners on the chip carrier base and positioned between the semiconductor die and said carrier base;

electrically conductive material interconnecting said semiconductor die bottom surface and at least one of said metallic runners through said pathway in said die pad.

9. The chip carrier assembly of claim 7, wherein said chip carrier base comprises ceramic alumina.

10. The chip carrier assembly of claim 7, wherein said electrically conductive material comprises silver filled epoxy.

11. The chip carrier assembly of claim 7, wherein said pathway comprises a punched hole therethrough said die pad positioned directly above said metallic runner.

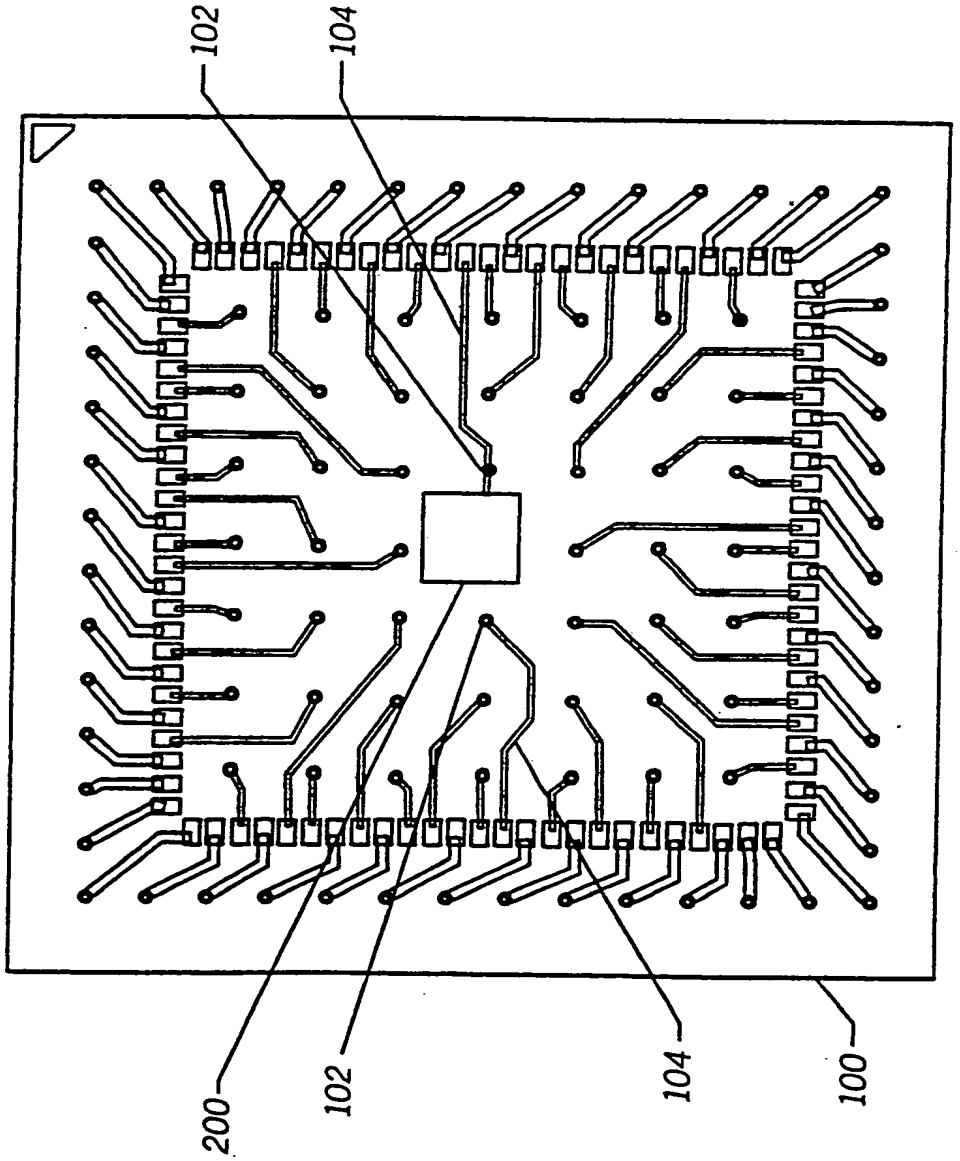


FIG.1

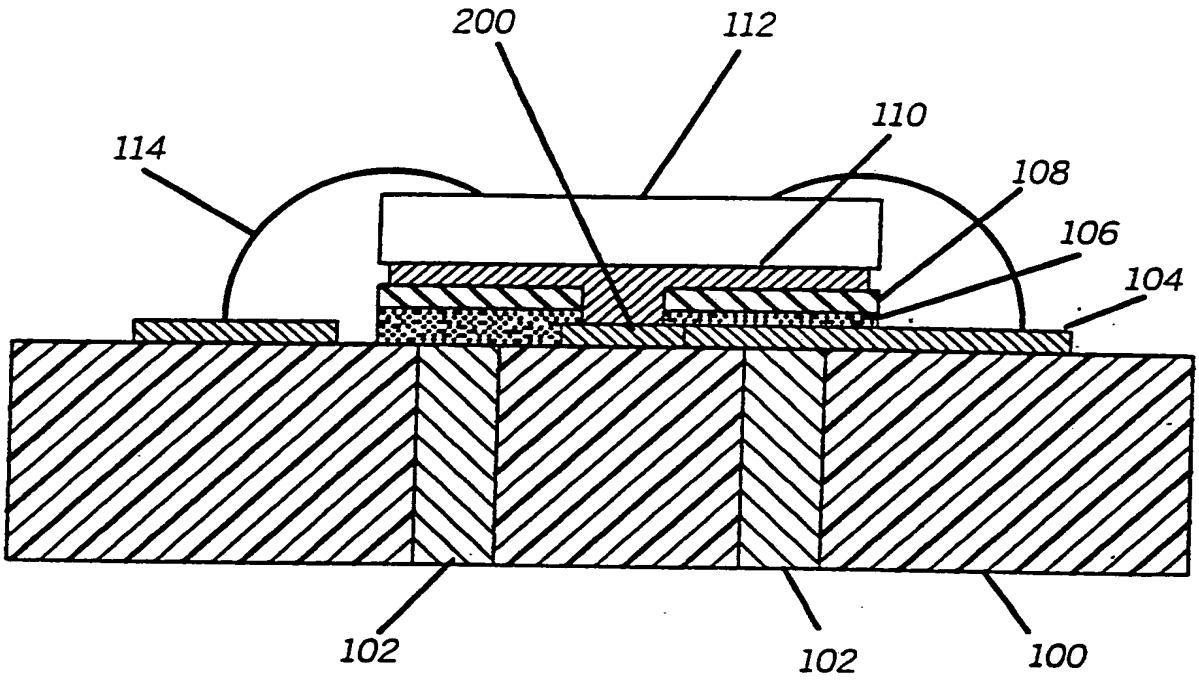
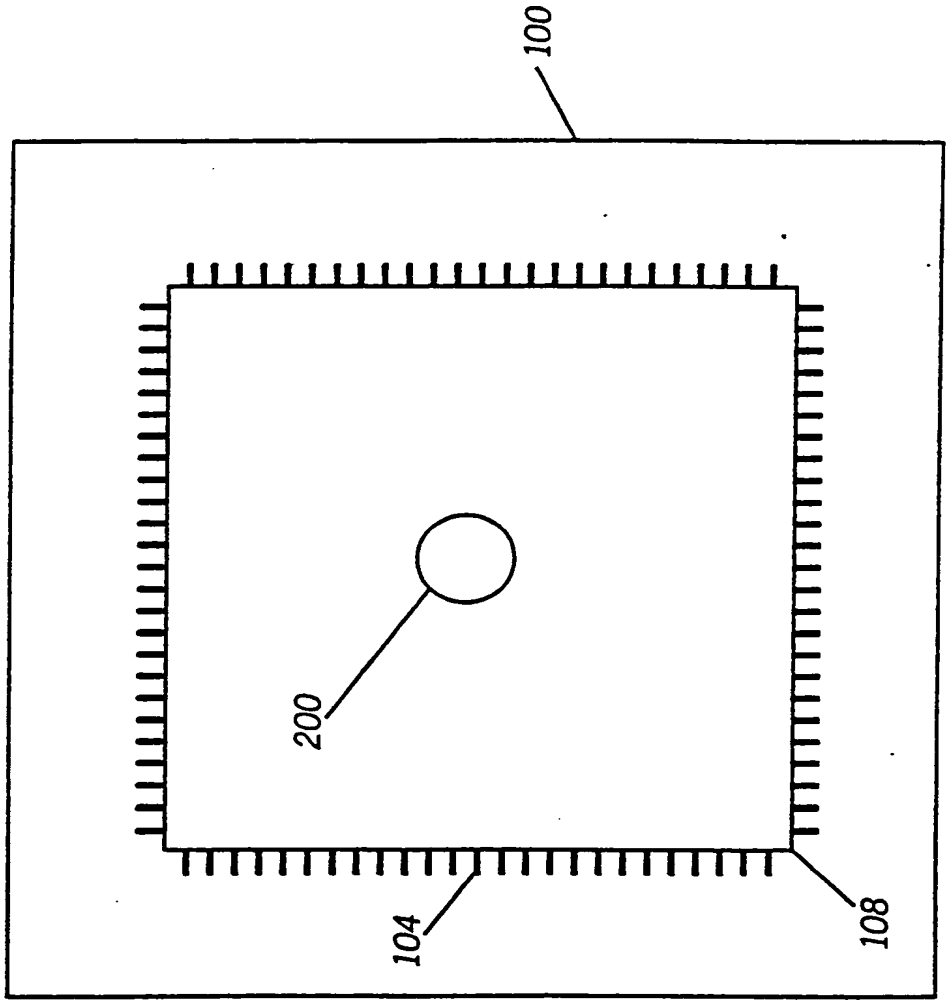


FIG.2

FIG.3



INTERNATIONAL SEARCH REPORT

International Application No. PCT/US90/01828

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): H05K 3/30 H01B 17/00 H01L 39/02 H05K 7/02: H05K 7/10
U.S. CL.: 29/832 174/138G 357/80 361/400,403

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	174/138G, 255,260 357/80 29/832 361/397, 400, 402, 403, 405, 406, 410, 414

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X Y	US, A, 4,631,639 (BIRAUD) 23 December 1986, See entire document.	1, 7 1-3,6,8-9
A	US, A, 4,574,879 (DeGREE ET. AL.) 11 March 1986, See entire document.	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
17 JULY 1990	14 AUG 1990

International Searching Authority	Signature of Authorized Officer
ISA/US	for GREG THOMPSON NGUYEN NGOC-HO INTERNATIONAL DIVISION

Form PCT/ISA/210 (second sheet) (Rev.11-87)